DETAILED ACTION

Response to Amendment

The Examiner acknowledges the amending of claims 1, 3, 7, and 12.

Response to Arguments

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

The Examiner comments that the Applicant's arguments on pgs.7-8 of the Remarks which states that the capacitor based circuit found in fig.1 #18 is not understood to have the currently amended limitations directed towards circuit layout. The Applicant further states that it is not understood that fig.1 #16 receives a signal which is an approximation of the average power of the duty cycle.

The Examiner firstly notes that the Applicant has not directly stated that the capacitor based circuit of #18 does not act to integrate, or average, the signal, but only that the claimed circuit layout is not present. The Examiner believes that the capacitor circuit does average the signal of #18 which is representative of the duty cycle voltage ([0006]). This is evidenced by the similar configuration of fig.5 #422 of the Specification wherein a capacitor is placed in parallel with the output of the previous circuit element. The capacitor of fig.1 is thought to act to integrate the voltage before it is sent to the op amp fig.1 #20. The Examiner does agree that the signal sent from #20 to #16 may not be an exact average power reading, but does in fact read on the limitation that the signal be "based, at least in part, on said average power signal".

The use of claim language such as "coupled" can be broadly interpreted in electrical applications. The Examiner suggests language such as "directly connected" to further define the electrical connections. Further it is noted that the language "based in part" is noted as being quite broad as to what the output signal is truly composed of.

Double Patenting

As discussed in the applicant's Remarks, pg.11, the provisional obviousness type double patenting rejection is stayed pending the outcome of the co-pending application No. 10/422829.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 7-8 are rejected under 35 U.S.C. 102(a) as being anticipated by the Applicant's admitted prior art (AAPA).

With respect to claim 7, the AAPA discloses a method comprising generating a pulse data output signal (fig.1 from #14) in response to an input signal (fig.1 at each gate of #12), the pulse data output signal comprising a duty cycle (SPEC pg.1 lines 21-22), receiving and integrating at a capacitor (fig.1 in #18) an amplified (relative term) signal from an output signal of an operational amplifier (fig.1 in #22, #22 outputs to #16

which changes the value on #24 which is received at the capacitor) to generate an average power signal approximating an average power of the pulse data output signal (see Response to Arguments above), and receiving at a first input terminal of a current steering device said average power signal (fig.1 #20) approximating to control the duty cycle of the pulse data output signal based, at least in part, on the average power signal.

With respect to claim 8, the AAPA discloses the laser driver as outlined in the rejection to claim 1, and further teaches the input stage to generate a differential signal on first and second terminals (fig.1 #24) coupled to the limiting amplifier (fig.1, to #14), and wherein the duty cycle circuit comprises a current steering circuit to apply an offset current to al least one of the first and second terminals (SPEC pg.1-2 lines 22-9) in response to the approximation of the average power of the pulse data output signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's admitted prior art (AAPA).

With respect to claim 1, the AAPA teaches a laser driver circuit comprising an input stage (fig.1 #12) to receive an input signal (fig.1 at each gate of #12), a circuit to generate a pulse data output signal (fig.1 #14) comprising a duty cycle (SPEC pg.1 lines 21-22), an output stage to modulate an output current signal based on the pulse data output signal (SPEC pg.1 lines 19-21), a duty cycle control circuit (fig.1 #16,18,22) comprising a capacitor (fig.1 in #18) coupled to a first input terminal of a current steering device (fig.1 #20, has a finite current output so can be considered "current steering") and an output terminal of an operational amplifier (fig.1 in #22), said capacitor configured to generate an average power signal approximating an average power of the pulse data output signal (see Response to Arguments above), wherein said current steering device is configured to receive said average power signal and to control the duty cycle of the pulse data output signal based, at least in part, on average power signal (in conjunction with #16). The AAPA does not teach the use of a limiting amplifier to generate the pulse data output signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to make use of a limiting amplifier to generate the pulse data output signal as the AAPA makes extensive use of amplifiers in the system, and the amplifier type is well known in the art to be used for current control techniques.

With respect to claim 2, the AAPA teaches the laser driver as outlined in the rejection to claim 1, and further teaches the input signal to comprise a bi-level signal (fig.1 bi-level input to #12).

With respect to claim 3, the AAPA teaches the laser driver as outlined in the rejection to claim 1, and further teaches the input stage to generate a differential signal on first and second terminals (fig.1 #24) coupled to the limiting amplifier (fig.1, to #14), and wherein the duty cycle circuit comprises a current steering circuit to apply an offset current to al least one of the first and second terminals (SPEC pg.1-2 lines 22-9) in response to the approximation of the average power of the pulse data output signal.

With respect to claim 18, the AAPA further teaches the average power approximation circuit is configured to maintain a voltage at an input terminal of the current steering circuit, the voltage representing the approximation of the average power of the pulse data output signal (fig.1, output of #18 to #20 and on to #16).

Claims 4-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA and further in view of Gilliland et al. (US 6711189).

With respect to claims 4 and 9, the AAPA teaches the laser driver as outlined in the rejection to claim 1, and further teaches a resistor pair located in the duty control circuit (1 pair in #16 and 1 pair in #18) to be used to set the control voltage which effects the duty cycle of the pulse data output signal. The AAPA does not teach the use of a potentiometer. Gilliland teaches a laser power control circuit in which a potentiometer is used to control an output voltage (abs. lines 4-5). It would have been obvious to one of

ordinary skill in the art at the time of the invention to combine the laser driver duty control circuit with the potentiometer of Gilliland in order to allow for adjustability of the resistance values and hence the controlling voltage.

With respect to claims 5-6 and 10-11, the AAPA and Gilliland teach the laser driver as outlined in the rejection to claims 4 and 9 above, and further teach the duty control circuit to comprise a differential amplifier (fig.1 FETs in #16) to generate a differential voltage on first and second terminals (fig.1 #24) in response to the pulse data output signal, and wherein the potentiometer (Gilliland's potentiometer) is coupled to the differential amplifier to determine a resistance between a voltage source (fig.1 VCC) and each of the first and second terminals.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA and further in view of Kenny (US 6654565).

With respect to claim 12, the AAPA teaches the laser driver outlined in the rejection to claim 1. The AAPA does not teach the laser driver to use a serializer. Kenny teaches a communication system utilizing a serializer (fig.9 #930). It would have been obvious at the time of the invention to combine the laser driver of the AAPA with the serializer of Kenny in order to implement the laser and driver into a high-speed system (Kenny, col.19 lines 56-60).

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA and Kenny, and further in view of Diaz et al. (US 6822987).

With respect to claim 13, the AAPA and Kenny teach the laser driving system as outlined in the rejection to claim 12, but do not teach the use of a SONET framer. Diaz teaches a high-speed laser array which uses a SONET framer (col.10 lines 46-48). It would have been obvious to one or ordinary skill in the art at the time of the invention to combine the laser driver system of the AAPA and Kenny with the SONET framer of Diaz in order to provide for high bit rate during very high speed applications (Diaz, col.9 lines 50-57).

With respect to claims 14-17, the AAPA, Kenny, and Diaz teach the laser system as outlined in the rejections to claims 12, and 13, while it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser system with a switch fabric coupled to the SONET, an Ethernet MAC and a multiplexed data bus since these components are well known and widely used in communications systems.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOD T. VAN ROY whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/TVR/

/Minsun Harvey/
Supervisory Patent Examiner, Art Unit 2828